Cadence SPB: What's New in 16.6 QIR 7 (HotFix 32)

This document describes the new features and enhancements in Cadence® SPB products in 16.6 Quarterly Incremental Release (QIR) 7- HotFix32. The products covered are:

- Allegro PCB Editor
- Cadence SiP Layout and Allegro Package Designer (APD)
- Allegro Design Entry HDL
- Allegro FPGA System Planner
- OrCAD Capture
- Cadence PSpice

Allegro PCB Editor

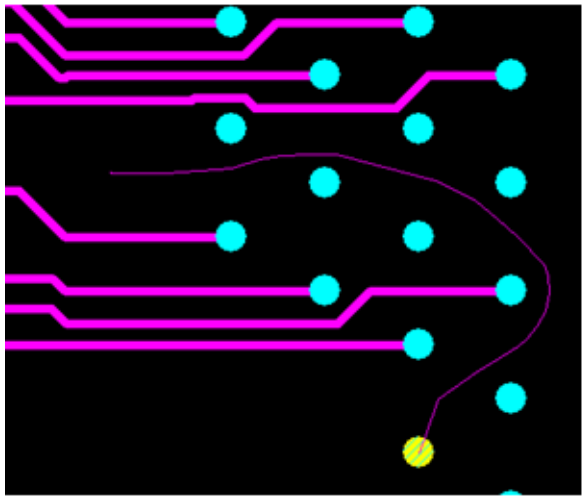
This document describes the new features and enhancements in Allegro® PCB Editor16.6 QIR 7.

Route Interconnect Optimization

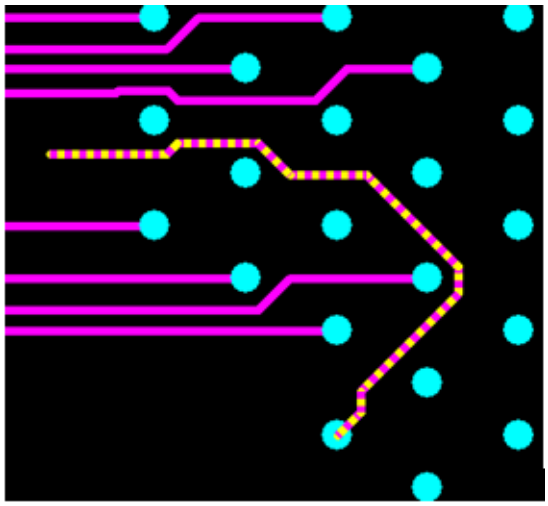
A major effort targeted at improving the productivity and efficiency of the interactive routing environment continues throughout the 16.6 incremental releases.

Scribble Mode Routing

Scribble is a simple routing mode that allows you to scribble a route path onto the canvas. Once a click is made, the etch solution for the scribble path will be generated. Scribble provides a quick two pick methodology to generate complex route paths, along with a very controlled usage of push/shove based on the scribble path.

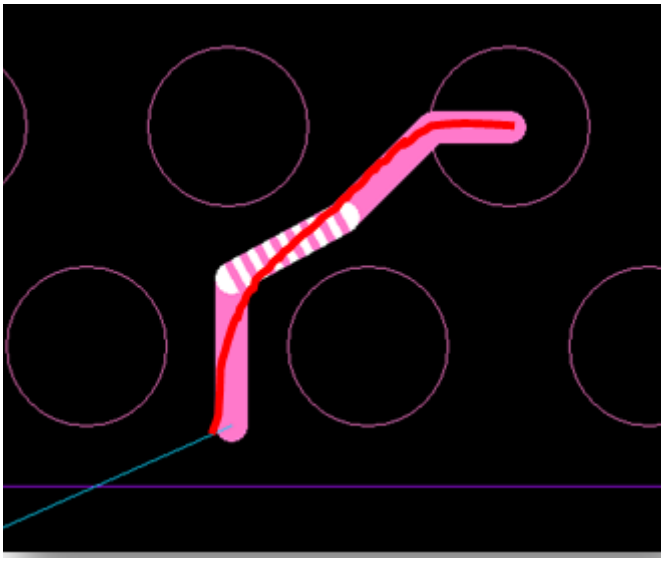


Scribble Path



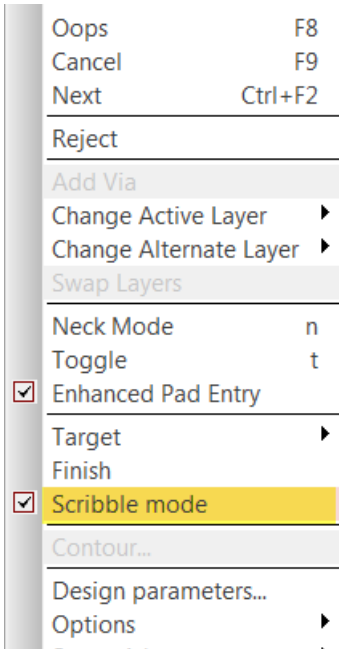
Route Results

An additional benefit of using scribble is its ability to navigate a routing path through pin pitches that require non-standard routing angles.



Off Angle Fit

Scribble mode is now available as a right-click menu of `add connect` command.



Tip

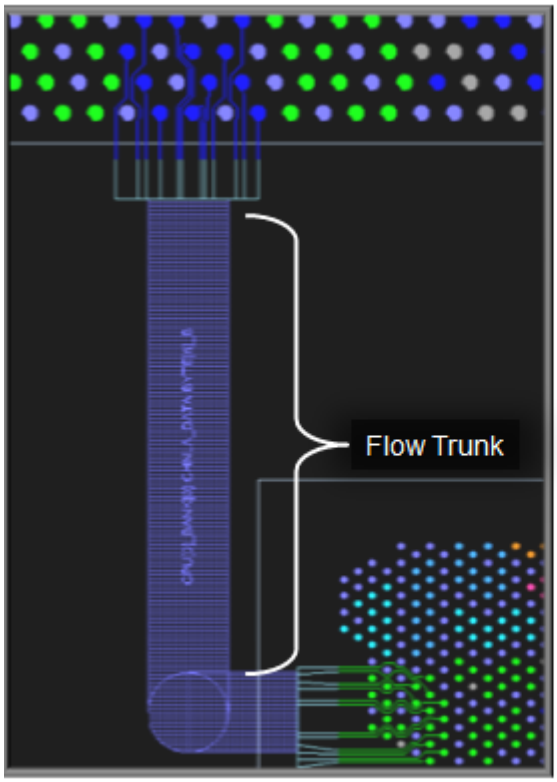
Use the `TAB` key to toggle scribble mode on/off during the `add connect` command.

For more information, see *About Scribble Mode* in *Allegro User Guide: Routing the Design*.

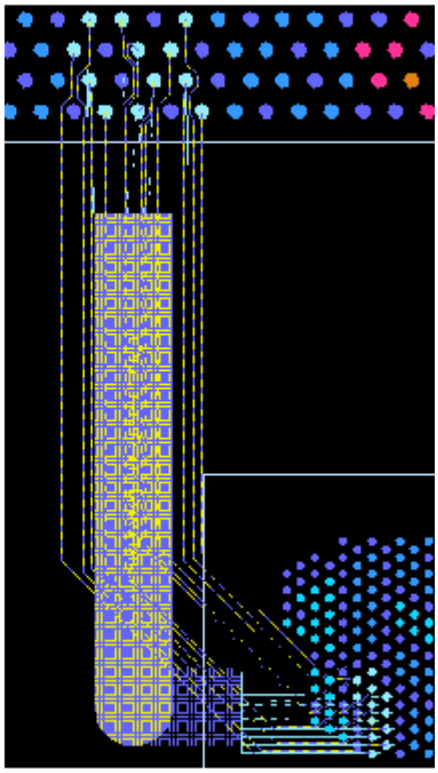
Auto-Interactive Trunk Route

Design Planning Option

The new Auto-Interactive command is designed to generate the interconnects between existing breakouts. After completion of component breakout routing, hover over any section of the bundle, right-click and choose *Auto – I. Route Trunk* command.



Breakout Patterns

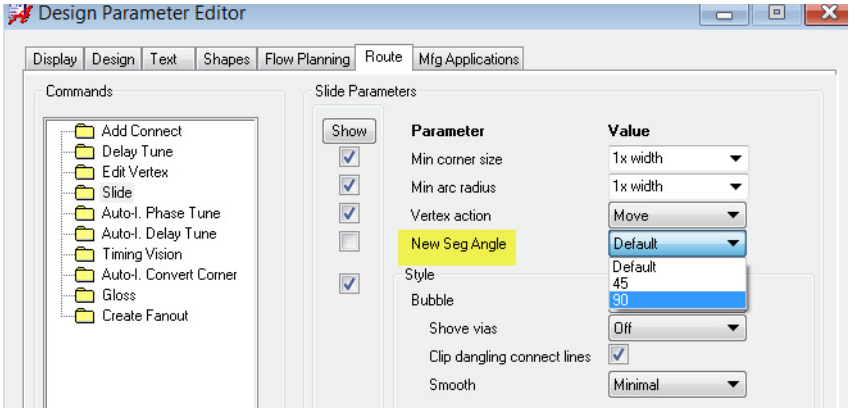


Trunk Route Results

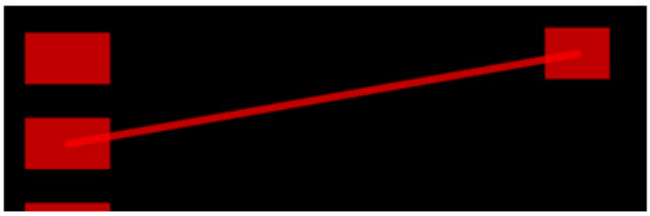
Slide Update

New Segment Angle Control

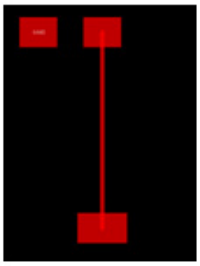
The `slide` command now supports a new option called *New Seg Angle*. This gives you more control over new segment construction. By default, this field is not visible in the *Options* tab. Browse to the *Route* tab of the *Design Parameter Editor* dialog box to either show the option or set the values.



The following image shows some examples of using the *New Seg Angle* option:

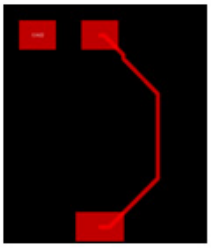


Start (off angle route)



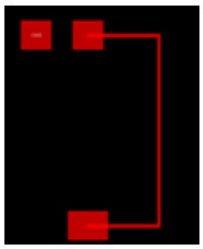
Start (straight route)

New Seg Angle = 45



New Seg Angle = default or 45

New Seg Angle = 90



New Seg Angle = 90

Productivity Enhancements

Unassigned Shapes Update

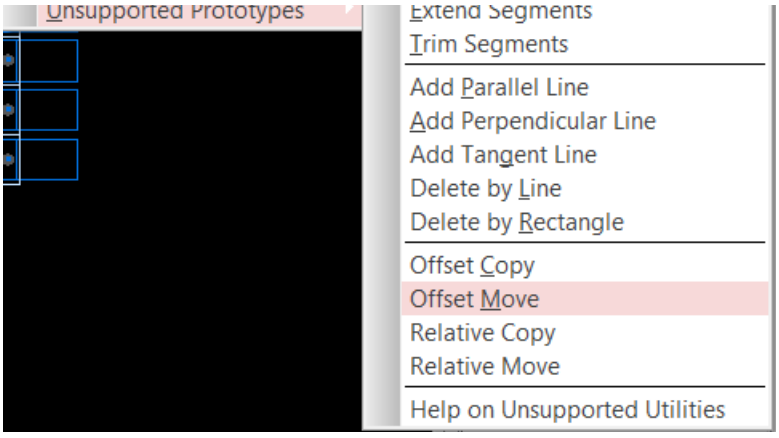
In a design with large number of NC pins it is difficult to navigate to real unassigned shapes. Starting from QIR 7, the NC pins assigned fillets will no longer be reported in the *Shapes Without an Assigned Net* report. This report is displayed when you choose *Unassigned shapes* button in the *Status* (*Display – Status*) dialog box.

Unsupported Prototype Functionality

You can use new functionalities that are currently in a prototype state but mature enough for use in production. The suite of commands is available in the *Unsupported Prototype* menu under the *Edit*, *View*, *Route* and *Manufacture* menus. Help document access is located on the last row of the menu.

Offset Move and Copy Update

Offset Move and *Offset Copy* are now part of a suite of drafting commands, currently available through the *Unsupported Prototype* menu. Offset values for both commands are now retained in the *Options* tab.



Misc. Enhancements

Bundle Visibility

Show All Bundles and *Blank All Bundles* commands are now available in common pop-up menu options in the *Etch Edit* application mode. To use these options enable *Groups* in the *Find* filter settings.

IDX update

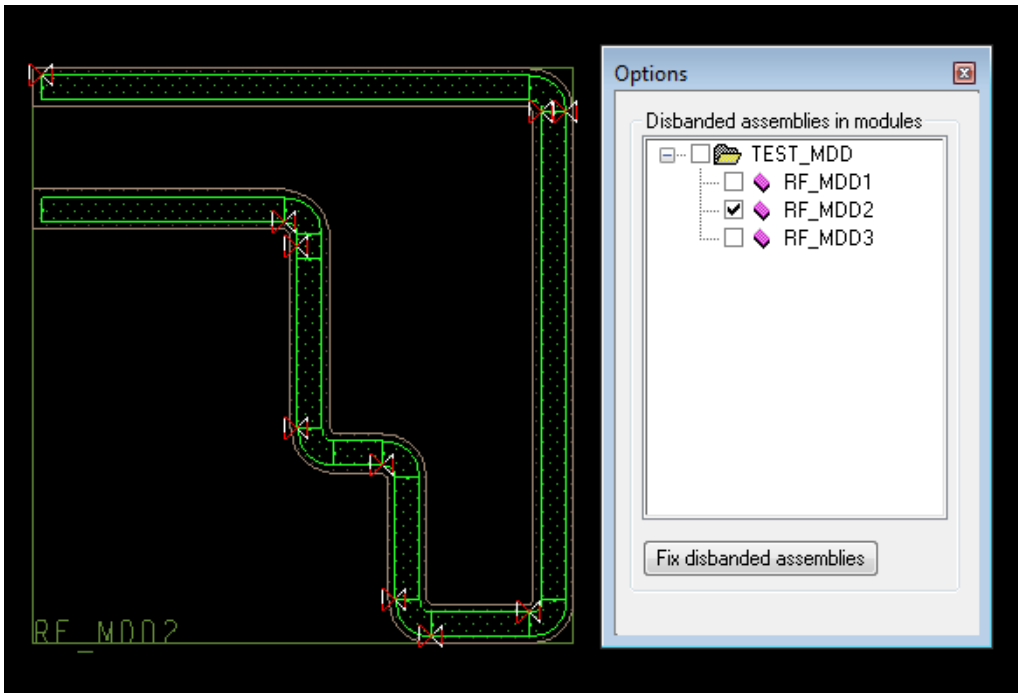
Orcad PCB Designer Standard now supports the *File – Export – IDX* command.

Product Choices

The *File – Change Editor* (`toolswap`) command has been enhanced to display all product choices. Prior to this release, the display was aligned with the product being opened.

RF PCB Enhancements

The placement of hard-reused modules with disbanded asymmetrical clearance assemblies leads to DRC errors of shape-to-route keepin spacing. In QIR 7, the `rf_ac_assemble` (*RF-PCB – Clearance – Assembly*) command has been enhanced to fix such modules by selecting them from the *Options* tab.



Cadence SiP Layout and Allegro Package Designer (APD)

This section describes the new features and enhancements in Cadence® SiP Layout and Allegro® Package Designer (APD) 16.6 QIR 7.

Note: The new features listed for Allegro PCB Editor on page 2 are also available from Cadence SiP Layout and Allegro Package Designer (APD).

Enhancements in the WLCSP Capabilities

QIR 7 has many new features that enhance the wafer-level-chip-scale-package (WLCSP) capability supported by the Cadence® packaging tools. The following enhancements and new features make the existing WLCSP flow even more efficient:

Adding Fully-Customized Components Directly in the Design

You can choose the *Add component* option in the Symbol Edit application mode to add fully customized components, starting from scratch, directly within the context of the package substrate design of the following types:

- Package
- Die
- Interposer
- Discrete
- Plating bar

Adding Fully-Customized and Complex Pin Patterns

You can quickly define a fully-customized and complex pin pattern, such as with multiple pitches, by selecting *Pattern definition* in the Options pane for the *Add pin* command in the Symbol Edit application mode.

Selecting *Pattern definition* shows the options that can be used to define a pattern and add the pattern to a group, enabling group operations on the set of pins. The pattern styles available are:

- *Single*: Place pins either by pick or by window. When windowing, the area will be filled with pins at the pitch specified for the grid in that area.
- *Array*: Place an array of pins with pitch specified in the Options pane.

- *Ring*: Place pins as rings, the pitch and numbers for which is specified in the Options pane.
- *Text File*: Create pins at a set of X and Y coordinates listed in the text file.
- *Spreadsheet*: Import pin pattern defined in a spreadsheet.

The different configuration options available on selecting the pattern styles allow flexible generation of pin patterns.

Converting Shapes, Vias, and Pins

Converting GDSII or DFX files into intelligent designs is now easy with the new conversion commands of SiP Layout and Allegro® Package Designer (APD). A set of commands available from the *Tools– Convert* menu convert shapes into clines, padstacks, and vias and are complemented by an option to convert pads to shapes. The options to convert vias to pins and pins to vias in the Symbol Edit application mode rounds off the enhancements in the conversion space.

The following new commands are available from the *Tools – Convert* menu:

- `pad to shape` (*Tools – Convert – Pad to Shape*): Copies specified pads of the selected pin, via, or finger to shapes on a selected layer.
- `shape to cline` (*Tools – Convert – Shape to Cline*): Converts specified shapes to clines.
- `shape to padstack` (*Tools – Convert – Shape to Padstack*): Converts shapes to padstacks, which are added to the physical constraint list.
- `shape to via` (*Tools – Convert – Shape to Via*): Converts shapes, lines, or clines to vias or bond fingers for which padstacks exist in the database. You have the option of converting all matching lines, clines, or shapes to vias or bond fingers.

The following options are available in the Symbol Edit application mode:

- *Convert pins to vias*: Creates vias matching the source pin's placement, padstack, and net assignments. You have the option of deleting (*Delete converted pins*) or retaining (*Keep converted pins*) the converted pins.
- *Convert vias to pin*: Creates pins for selected vias using the padstack, location, rotation, and net name of the vias. You have the option of deleting (*Delete converted vias*) or retaining (*Keep converted vias*) the converted vias.

Importing Pin Numbers and Nets While Composing Symbol from Geometry

You can now create pin numbers and nets based on imported geometry data using the new options, *Import Pin numbers* and *Import Nets* of the *Compose Die From Geometry* dialog box (*Add – Standard Die – Compose From Geometry*).

Importing Symbol Spreadsheet

The `spreadsheet to symbol` command (*File – Import – Symbol Spreadsheet*) lets you import information from a standard spreadsheet tool such as Microsoft Excel to update a placed component. You can use this command to exchange information with your system architect, front-end tools, or as part of your manufacturing documentation set when signing off a design. Use this command along with the existing `symbol to spreadsheet` command (*File – Export – Symbol Spreadsheet*) to update changes between various designers working on a symbol.

Note: This command supports updating information of existing pins only. You cannot add or delete pins using this command.

Aligning Vias

The *via align* command (*Route – Resize/Respace – Align Vias*) aligns selected vias in both vertical and horizontal directions according to the following placement options:

- Vertical placement options are:
  - *None*
  - *Top*
  - *Center*
  - *Bottom*
  - *Evenly Spaced*
- Horizontal placement options are:
  - *None*
  - *Left*
  - *Center*

- *Right*
- *Evenly Spaced*

Renaming Existing Padstacks

Now you can use the `rename padstack` (*Tools – Padstacks – Rename)* command to change the name of existing padstacks in a design. This command changes the following for the changed padstack name: all references in constraint via lists; all via, bond finger, and pin references to the padstack; and stored name mappings.

Note: The `rename padstack` command will not update the `.pad` file in your library. If you are updating the padstack for a symbol pin, the definition will be updated as well. As a result, a refresh of symbols on that drawing would reset it to the original name, as the library symbol would need to be manually updated.

Calculating Minimum Air Gap

Use the `calc min airgap` command (*Display – Min Airgap*) to calculate the minimum air gap for selected items on specified layers. You can select to calculate air gap between pins, vias, fingers, clines, lines, shapes and so on.

The air gap is displayed in the Options pane window and a line is shown between the objects for which the air gap is being calculated.

Enhancement to the Respace Option of Symbol Edit Application Mode

Earlier, the Respace option of the Symbol Edit application mode allowed only a pin to be selected for respacing as a reference; all the pins are than respaced relative to the reference pin. Now, you can select a reference point other than the pins selected for respacing. For example, you can select the center of a symbol as the reference point to avoid pins moving out beyond the symbol extents. Following should be noted:

- The pitch is calculated based on the selected pins – only respacing is performed relative to the selected reference point.
- If you select a pin as a reference, it must be part of the set of pins that you are respacing.

Allegro Design Entry HDL

This section describes the new features and enhancements in Allegro® Design Entry HDL 16.6 QIR 7.

Hierarchical Split Symbol Editing

A new dialog box, Customize Symbol Graphics, in Allegro Design Entry HDL now provides you the ability to specify the location and position for ports in each hierarchical split symbol of your design. This new dialog can be accessed from the Distribute Port dialog box. For more information, see the Working with Hierarchical Split Symbols section in *Allegro Design Entry HDL User Guide*.

Support for Logical Component Browser in Variant Editor

The logical Component Browser is now supported in Variant Editor. When you select a part to be replaced in Variant Editor, the Replace Component dialog box opens, which displays all the libraries and components in your design instead of only those libraries from which parts were selected in the schematic.

The Replace Component dialog box is essentially the Component Browser, which lets you search and select library parts defined in your design. You can search for parts, view details of parts including symbols and footprint, and replace parts.

SHOW_PNN_SIGNAME for Bus Objects

Selecting this option in DE HDL displays the physical net name for scalar signals and the bus name for vector buses.

Performance Improvements in ECSet Audit

The 16.6 QIR 7 release contains performance improvements for ECSet audits.

Allegro FPGA System Planner

This section describes the new features and enhancements in Allegro® FPGA System Planner16.6 QIR 7.

Name Based Power Mapping

In the current release, FSP introduces a new power mapping method. In this method, you map a power pin name to a power regulator. For example, you define a power regulator, *V_1_5,* of voltage value 1.5 v. To connect *V_1_5* to all the power pins of an instance that are powered by 1.5 v, map the power pin name to *V_1_5.*

You can also add two power regulators of the same voltage value with different names, and map them to different power pins that are powered by the same voltage. For example, you add two power regulators: *V_1_2_N* and *V_1_2_P.* Now, you can map a power pin name to *V_1_2_N* and another different power pin name to *V_1_2_P.*

Additional Enhancements

Significant enhancements have been made in the following sections:

- A new view, *Graphics View* is introduced in the *Schematic Symbol Editor.* The Graphics view provides you a graphical view of a symbol group/bank. You can also use this graphics view to view the changes that you make in the Tree view. Besides visualizing, you can change the pin direction of a pin by using a drag-and-drop operation. In addition, the *Schematic Symbol Editor* form maintains the association between the Tree view and Graphics view. When you make any changes in the Tree view the changes are immediately updated in the Graphics view as well. Similarly, when you make any changes in the Graphics view, the changes are also updated in the Tree view.
- In the current release, you can now select a symbol version while placing a component through Component Browser.
- A new option is added in the *Generate OrCAD Schematics* dialog box. This option can be used to name the vectored signals as *MSB* to *LSB* or *LSB* to *MSB.*
- You can now restore the toolbar settings to their default settings using *Restore Defaults* in the *Customize Toolbar* dialog box.
- In the current release, you can now import the constraints from a .pin file for Altera FPGAs; however exporting the constraints to the .pin file is not supported.
- In *Process Options Editor,* you can now save, load, and delete the process settings.

A powerful filter and search pane, *Device Region* is introduced in the Die View using which you can filter or search for a specific bank or region name. The *Device Region* pane also provides a list of bank numbers and region names of the device that is placed on the Canvas. You can click on the region names to navigate to the pins that are present in the region you have selected.

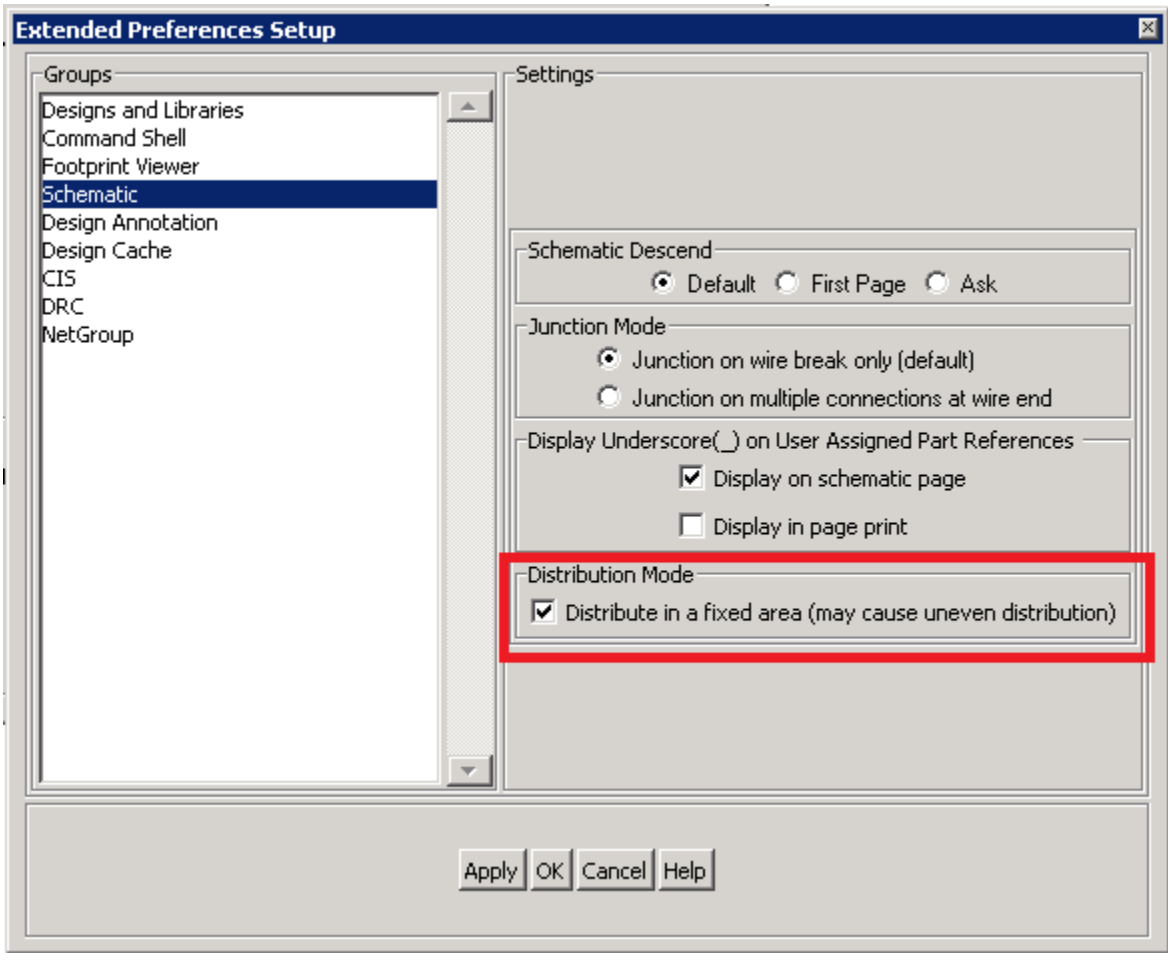
OrCAD Capture

This section describes the new features and enhancements in OrCAD® Capture 16.6 QIR 7.

Enhancements in the Object Distribution Feature

Prior to 16.6 QIR7, you could distribute the selected Capture objects horizontally or vertically within a virtual selection bounding box. The distribution, using the Object Distribution feature, was occurring in a fixed area.

From 16.6 QIR7, you can distribute the selected capture objects horizontally or vertically within a virtual selection bounding box, but the bounding box might be compressed or expanded.

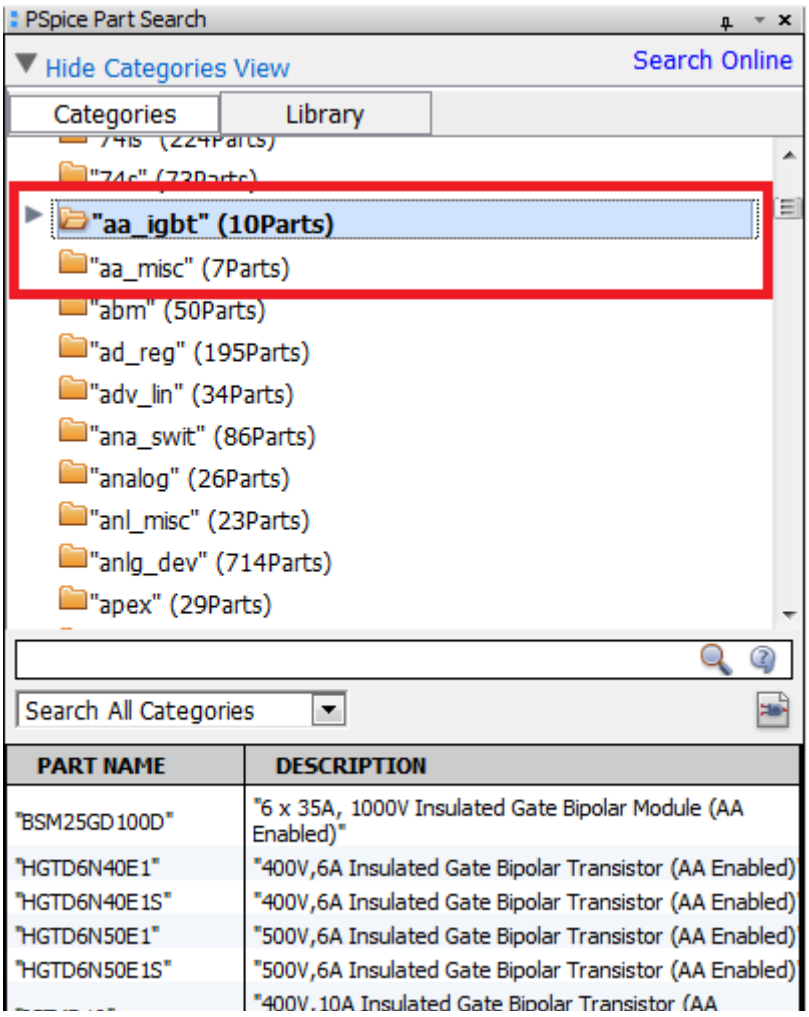


By default, the *Distribute in a fixed area* check box in the Schematic section of the Extended Preferences Setup window is unchecked. This window can be accessed from *Accessories — Cadence Tcl/Tk Utilities — Utilities — Tcl/Tk Applications Dashboard*. If the check box is unchecked, the Capture objects are distributed in a virtual selection bounding box, which might be expanded or compressed.

Note: If you want to distribute the objects in a fixed area, click the *Distribute in a fixed area* check box.

Enhancements in PSpice Part Search

Now, PSpice Advance Analysis libraries, such as, `aa_igbt.olb`, `function.olb`, and so on, are also added to the PSpice Part Search database.

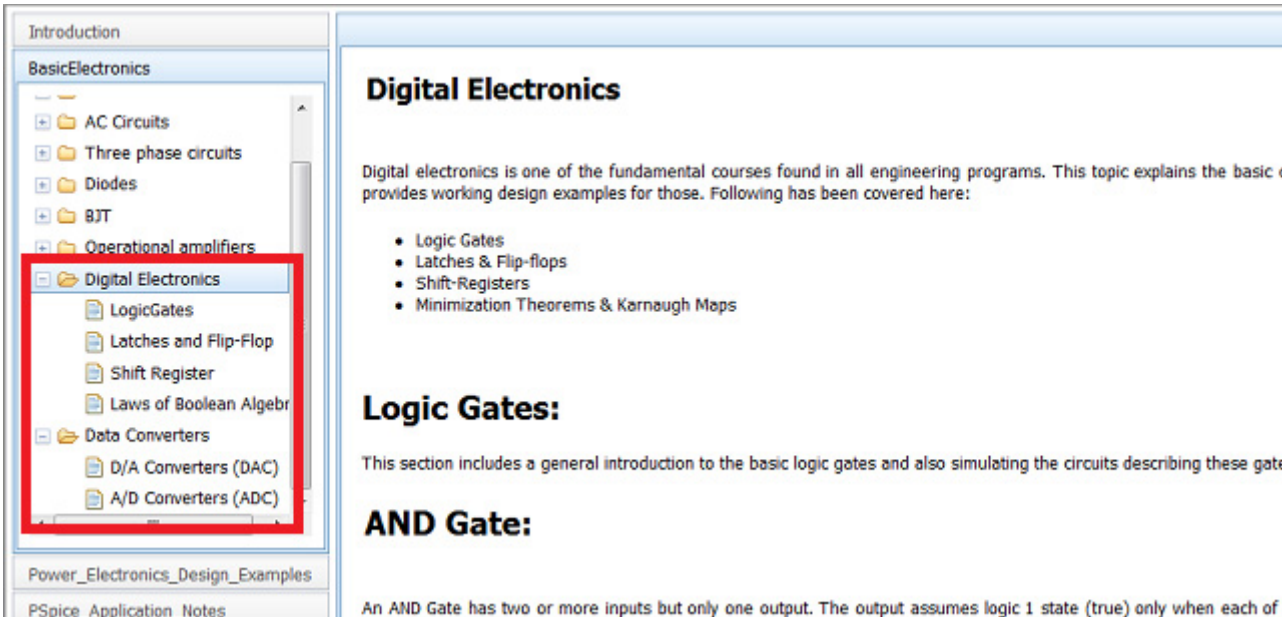


You can search the PSpice Advance Analysis parts using PSpice Part Search and place them in your designs.

The PSpice Advance Analysis parts are also categorized according to their function in PSpice Part Search's Categories tab.

Enhancements in Learning PSpice

Two new chapters have been added to the Basic Electronics book in Learning PSpice. These chapters explain digital electronics and data convertors using working examples.



Digital Electronics chapter covers the following topics:

- Logic Gates
- Latches and Flip-flops
- Shift Register
- Minimization Theorems and Karnaugh Maps

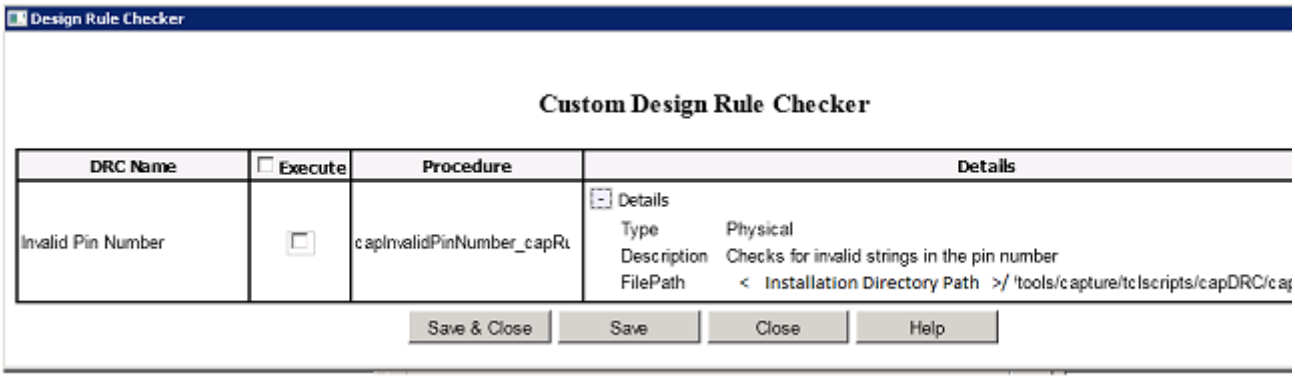
The Data Convertors chapter covers the following topics:

- Digital-To-Analog Converters (DAC)
- Analog-to-Digital Converter (ADC)

Note: You can access Learning PSpice only in Capture–PSpice flow. To access Learning PSpice, choose `Help — Learning PSpice` in Capture.

Enhancements in Custom Design Rule Checker

A new Design Rule Check (DRC), *Invalid Pin Number*, has been added under Physical DRC to check invalid string in pin numbers in 16.6 QIR7.



Capture, with Invalid Pin Number DRC enabled, checks if the following characters are present in the pin number: Exclamation (`!`), Backslash (`\`), Apostrophe (`'`). If these invalid characters exist in the pin number, Capture raises a DRC.

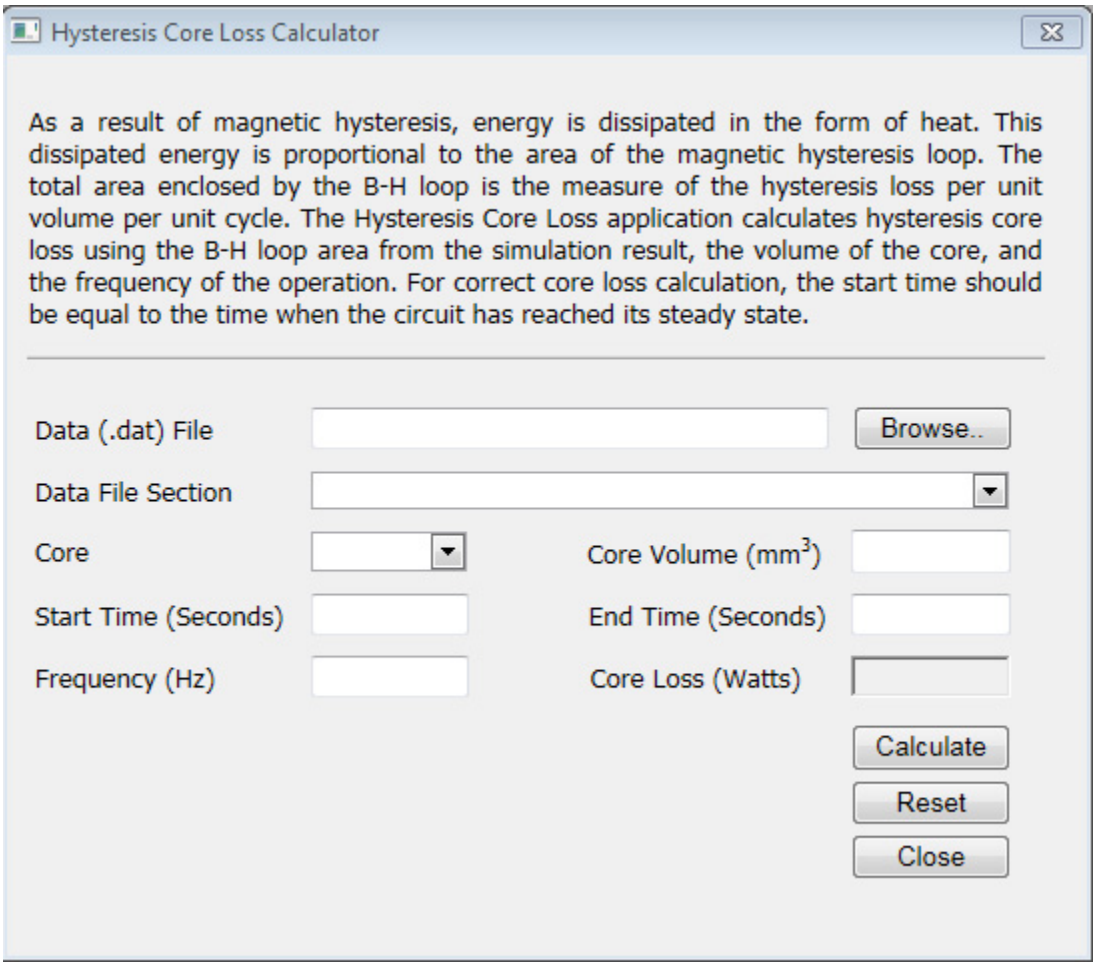
You can also add your own invalid strings by modifying the TCL file (`capInvalidPinNumber.tcl`) file located at `<Installation Path>\tools\capture\tclscripts\ capDRC`.

Cadence PSpice

This section describes the new features and enhancements in Cadence® PSpice® 16.6 QIR 7.

Hysteresis Core Loss Calculator

From 16.6 QIR7, PSpice provides you a Hysteresis Core Loss Calculator to calculate the area of the B-H curve, which is the integrated average of B-H loops, on the basis of the specified time range, that is, the start time and end time.



To calculate the hysteresis core loss of the core, you need to specify the following:

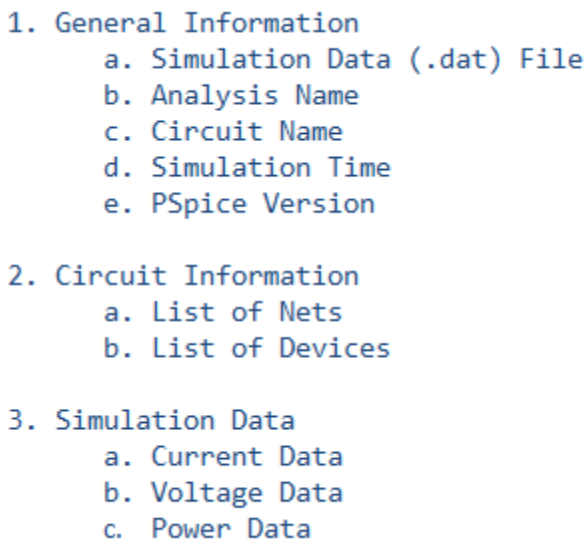
- time range, that is, the start time and end time
- frequency of the operation
- volume of the core

You can access Hysteresis Core Loss Calculator from *Tools — PSpice Calculator — Hysteresis Core Loss.*

Note: For accurate core loss calculation, specify a value for the maximum step size that generates optimal number of data points.

PSpice Report

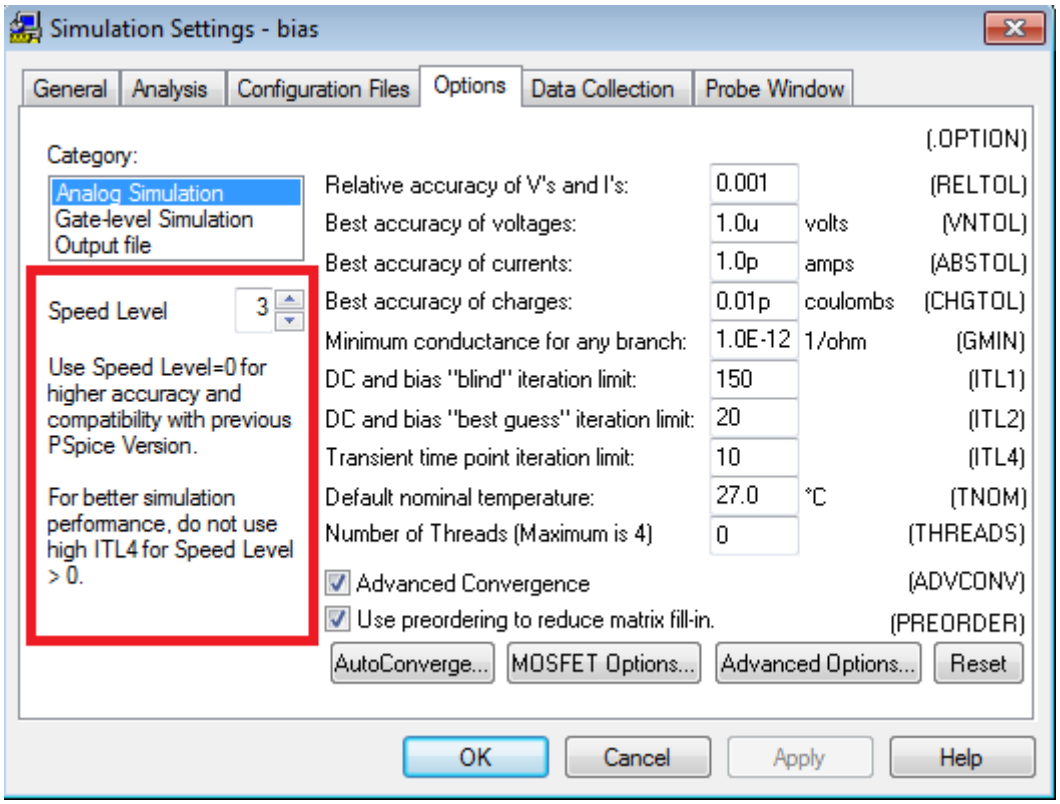
The Generate Report option, which can be accessed from *Tools — Generate Report*, generates an HTML report of the transient analysis data. The following figure shows the template of the HTML report:



You can modify the template by modifying the TCL (`orPspReport.tcl`) file, which is located at the following path: `<Installation Directory>\tools\pspice\tclscripts`.

PSpice Performance Upgrade

A new option, `Speed_Level`, has been added in the Simulation Settings GUI to enhance the simulation performance.

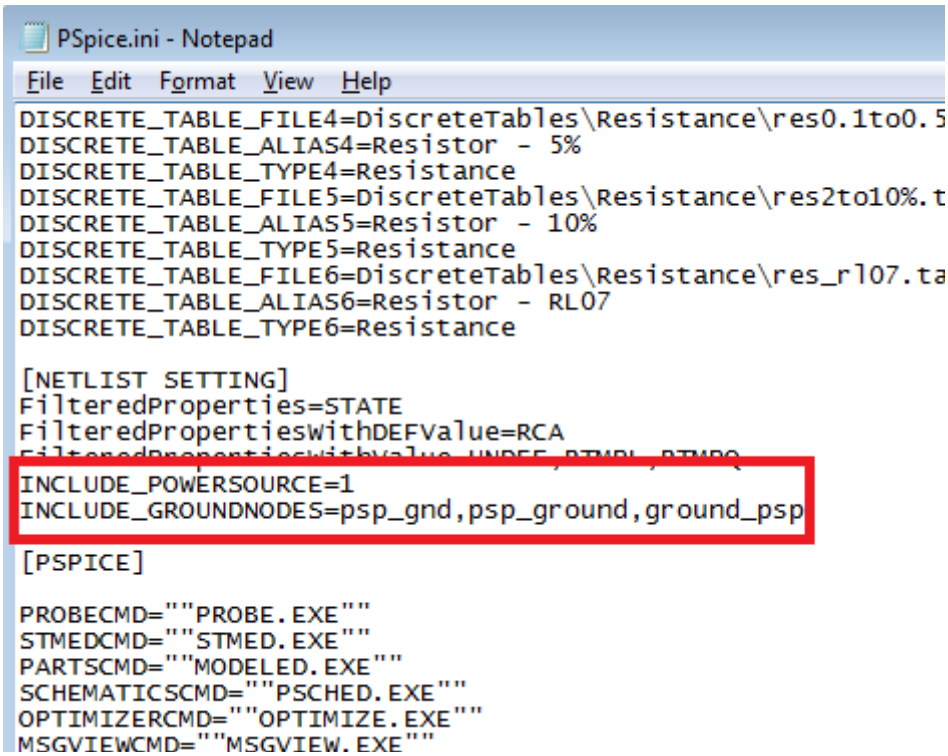


The `speed_level` option increases the simulation performance by optimizing the switching behavior of models. The value range of this option is from 0 to 5. The default value for this option is 3.

If performance enhancement is not required, set value 0 for this option.

Design Entry HDL power symbols support in the DE HDL-AMS Simulator flow

From 16.6 QIR 7, AMS simulator supports Design Entry HDL power symbols in the DE HDL-AMS Simulator flow.



The following points describe the use of the DEHDL power sources in the DE HDL-AMS Simulator flow:

- A power symbol that has the `HDL_POWER` and `VOLTAGE` property defined can be netlisted as a voltage source by enabling a flag in PSpice.ini. The flag contains a keyword, `INCLUDE_POWERSOURCE`, which should be equal to one. This flag should be added in PSpice.ini under the [NETLIST SETTING] section.
- A power symbol that has the `HDL_POWER` property and the `VOLTAGE` property, which is equal to zero, is netlisted as ground source in DE HDL-AMS Simulator flow.
- To enable user-defined ground names as valid ground sources in DE HDL-AMS Simulator flow, define a flag in PSpice.ini under the [NETLIST SETTING] section. The flag contains a keyword, `INCLUDE_GROUNDNODES`, which should have comma-separated user-defined ground names.

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Two new chapters have been added to the Basic Electronics book in Learning PSpice. These chapters explain digital electronics and data convertors using working examples.

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